CLAIMS

What is claimed is:

1. A system to limit a maximum duty cycle of a pulse-width modulated (PWM) signal, comprising:

circuitry that provides a clamp waveform based at least in part on a first reference signal;

a comparator that compares the clamp waveform relative to a reference waveform to provide a limiting signal, the reference waveform is based at least in part on a second reference signal, such that the limiting signal has a duty cycle functionally related to the first and second reference signals, whereby application of the limiting signal to the PWM signal limits the PWM signal to within a maximum duty cycle.

2. The system of claim 1, further comprising a first reference component that defines the first reference signal and a second reference component that defines the second reference signal, at least one of the first and second reference components being programmable to set the duty cycle of the limiting signal.

3. The system of claim 2, the first and second reference components comprising respective first and second resistors.

4. The system of claim 1, at least one of the first and second reference signals being variable so that the duty cycle of the limiting varies as a function of the variable one of the first and second reference signals, whereby the system operates as a volt-second clamp.

5. The system of claim 1, the circuitry further comprising a capacitor coupled to generate the clamp waveform based on selective application of at least one of the first and second reference signals relative to the capacitor.

6. The system of claim 5, the circuitry further comprising at least one switch coupled to selectively provide at least the second reference signal relative to the capacitor based on the limiting signal and the PWM signal.

7. The system of claim 6, further comprising clamp circuitry coupled to the capacitor and operative, based on the state of the at least one switch, to modify the clamp waveform to limit the PWM signal to a transient duty cycle that is incrementally greater than the maximum duty cycle, whereby a rapid duty cycle limit convergence time is facilitated.

8. An integrated circuit comprising the system of claim 1, the integrated circuit further comprising a waveform generator that generates the reference waveform.

9. The integrated circuit of claim 8,

the waveform generator generates the reference waveform to have a waveform characteristic as a function of least a first component thereof,

the circuitry generates the clamp waveform to have a waveform characteristic as a function of at least a second component, the first and second components being substantially matched components in the integrated circuit.

10. The integrated circuit of claim 9, the first and second components further comprising respective first and second capacitors.

11. The integrated circuit of claim 10, further comprising at least one switch coupled to selectively provide at least the second reference signal relative to second capacitor based on the limiting signal and the PWM signal.

12. The integrated circuit of claim 9, the waveform generator generating the reference waveform to have a frequency based on one of a predetermined peak threshold level and a synchronization signal.

13. The integrated circuit of claim 8, further comprising a first resistor that defines the first reference signal and a second resistor that defines the second reference signal, at least one of the first and second resistors being external to the integrated circuit and programmable to set the duty cycle of the limiting signal.

14. A system to limit a maximum duty cycle of a pulse-width modulated (PWM) control signal, comprising:

a waveform generator that provides a reference waveform based on a first reference signal; and

a clamp system that generates a clamp waveform based on the first reference signal and a second reference signal, the clamp system providing a limiting signal based on the reference waveform relative to the clamp waveform, such that the limiting signal can be applied to limit the duty cycle of the PWM signal.

15. The system of claim 14,

the waveform generator further comprising a first component that provides the reference waveform based on application of the first reference signal relative to the first component; and

the clamp system further comprising a second component that provides the clamp waveform based on application of the first and second reference signals relative to the second component.

16. The system of claim 15, the first and second components further comprising substantially matched capacitors.

17. The system of claim 15, further comprising at least one switch coupled to selectively provide at least the second reference signal relative to the capacitor of the clamp system based on the limiting signal and the PWM signal.

18. The system of claim 14, further comprising a first resistor that defines the first reference signal and a second resistor that defines the second reference signal, at least one

of the first and second resistors being programmable to set the duty cycle of the limiting signal.

19. The system of claim 14, the limiting signal having an on-time and an off-time during each period thereof, the reference waveform and the clamp waveform having substantially proportional slopes during the off-time of periods for the limiting signal.

20. An integrated circuit comprising the system of claim 14.

21. A system to limit a maximum duty cycle of a pulse-width modulated (PWM) control signal, comprising:

means for generating a reference waveform based on a first reference signal;

means for generating a clamp waveform based on at least a second reference signal;

means for providing a limiting signal based on a comparison of the reference waveform and the clamp waveform; and

means for applying the limiting signal to limit the duty cycle of the PWM signal according to the duty cycle of the limiting signal, which is functionally related to the first and second reference signals.

22. The system of claim 21, further comprising means for programming at least one of the first and second reference signals.

23. The system of claim 21, the reference waveform generating means and the clamp waveform generating means including matched capacitors that operate to provide the respective reference and clamp waveforms.

24. A method for limiting a maximum duty cycle of a pulse-width modulated (PWM) signal, comprising:

receiving a reference waveform based on a first reference signal;

generating a clamp waveform based on a second reference signal and the first reference signal; and

comparing the reference waveform relative to the clamp waveform to provide a limiting signal having a duty cycle functionally related to the first and second reference signals, whereby application of the limiting signal to the PWM signal limits the duty cycle of the PWM signal.

25. The method of claim 24, further comprising programming the second reference signal based on a resistive component.

26. The method of claim 25, further comprising:

programming the first reference signal by coupling a first external resistive component to an integrated circuit operative to implement the method; and

programming the second reference signal by coupling a second external resistive component to the integrated circuit, such that the maximum duty cycle is set as a function of the first and second resistive components.

27. The method of claim 26, the reference waveform being generated based on application of the first reference signal to a first capacitor, the clamp waveform being generated based on application of the first and second reference signals to a second capacitor, the first and second capacitors being substantially matched capacitors in the integrated circuit.